CLAIMS

What is claimed is:

1. A method of using a transient voltage suppression device, comprising:

electrically coupling gate and drain terminals of a metal oxide semiconductor device;

clamping a forward voltage applied across the transient voltage suppression device to be substantially equal to a threshold potential of the metal oxide semiconductor device; and

clamping a reverse voltage applied across the transient voltage suppression device to be substantially equal to a barrier potential of the metal oxide semiconductor device.

2. The method of claim 1 wherein clamping the forward voltage comprises:

applying a first potential of a first polarity to the gate and drain terminals of the metal oxide semiconductor device; and

producing a first conductive state of the metal oxide semiconductor device with the first potential.

3. The method of claim 2 wherein clamping the reverse voltage comprises:

applying a second potential of a second polarity to the gate and drain terminals of the metal oxide semiconductor device; and

producing a second conductive state of the metal oxide semiconductor device with the second potential.

4. A method of forming a transient voltage suppression device, comprising:

electrically coupling gate and collector terminals of an insulated gate bipolar transistor device;

clamping a forward voltage applied across the transient voltage suppression device to be substantially equal to a threshold potential of the insulated gate bipolar transistor device; and

clamping a reverse voltage applied across the transient voltage suppression device to be substantially equal to a barrier potential of the insulated gate bipolar transistor device.

5. The method of claim 4 wherein clamping the forward voltage comprises:

applying a first potential of a first polarity to the gate and collector terminals of the insulated gate bipolar transistor device; and

producing a first conductive state of the insulated gate bipolar transistor device with the first potential.

6. The method of claim 5 wherein clamping the reverse voltage comprises:

applying a second potential of a second polarity to the gate and collector terminals of the insulated gate bipolar transistor device; and

producing a second conductive state of the insulated gate bipolar transistor device with the second potential.

7. A method of using a transient voltage suppression device, comprising:

electrically coupling gate and drain terminals of first and second metal oxide semiconductor devices;

clamping a forward voltage applied across the transient voltage suppression device to be substantially equal to a first threshold potential of the first metal oxide semiconductor device; and

clamping a reverse voltage applied across the transient voltage suppression device to be substantially equal to a second threshold potential of the second metal oxide semiconductor device.

8. The method of claim 7 wherein clamping the forward voltage comprises:

applying a first potential of a first polarity to the gate and drain terminals of the first metal oxide semiconductor device; and

producing a first conductive state of the first metal oxide semiconductor device with the first potential.

9. The method of claim 8 wherein clamping the reverse voltage comprises:

applying a second potential of a second polarity to the gate and drain terminals of the second metal oxide semiconductor device; and

producing a second conductive state of the second metal oxide semiconductor device with the second potential.

10. A metal oxide semiconductor device used as a transient voltage suppressor, the transient voltage suppressor comprising:

a semiconductor substrate having first and second surfaces;

a body region of a first conductivity type formed in the first surface of the semiconductor substrate having first and second surfaces;

a drain region of a second conductivity type formed in the second surface of the semiconductor substrate; and

a trench gate region formed in the first surface of the semiconductor substrate.

11. The metal oxide semiconductor device of claim 10 wherein the transient voltage suppressor further comprises source regions of the second conductivity type formed in the first surface of the body region.

12. The transient voltage suppressor of claim 10 wherein the trench gate region extends from the first surface of the semiconductor substrate into the drain region.

13. The transient voltage suppressor of claim 12 wherein the trench gate region comprises an insulative layer within the trench gate region extending from the first surface of the semiconductor substrate to below the second surface of the body region.

14. The transient voltage suppressor of claim 11 further comprising a source metal layer on the first surface of the semiconductor substrate providing an electrical contact to the first and second source regions.

15. An insulated gate bipolar transistor device used as a transient voltage suppressor, the transient voltage suppressor comprising:

a semiconductor substrate having first and second surfaces;

a body region of a first conductivity type formed in the first surface of the semiconductor substrate having first and second surfaces;

a collector region of the first conductivity type formed in the second surface of the semiconductor substrate; and

a trench gate region formed in the first surface of the semiconductor substrate.

16. The insulated gate bipolar transistor device of claim 15 wherein the transient voltage suppressor further comprises emitter regions of a second conductivity type formed in the first surface of the body region.

17. The transient voltage suppressor of claim 15 wherein the trench gate region extends from the first surface of the semiconductor substrate into the drain region.

18. The transient voltage suppressor of claim 15 wherein the trench gate region comprises an insulative layer within the trench gate region extending from the first surface of the semiconductor substrate to below the second surface of the body region.

19. The transient voltage suppressor of claim 16 further comprising a source metal layer (74)on the first surface of the semiconductor substrate providing an electrical contact to the first and second emitter regions.

20. A protection circuit, comprising:

a utilization circuit (2)having an input coupled to receive an input signal at a first node; and

a protection circuit coupled to the first node to substantially limit the input signal to a first level, the protection circuit including

a transistor having a first conductor coupled to a control terminal of the transistor at the first node.

21. The protection circuit of claim 20, wherein the transistor includes a metal oxide semiconductor having a second conductor coupled to a second node.

22. The protection circuit of claim 21 wherein the metal oxide semiconductor device comprises:

a semiconductor substrate having first and second surfaces;

a body region of a first conductivity type in the first surface of the semiconductor substrate;

source regions of a second conductivity type formed in the body region;

a gate electrode formed over the first surface of the semiconductor substrate partially overlapping the source regions;

a drain region of the second conductivity type formed in the second surface; and

an electrical conductor coupling the gate electrode and the drain region.

23. The protection circuit of claim 21 wherein the metal oxide semiconductor device comprises:

a semiconductor substrate having first and second surfaces;

a source region of a first conductivity type formed in the first surface;

a drain region of the first conductivity type formed in the first surface;

a gate electrode formed over the first surface of the semiconductor substrate partially overlapping the source and drain regions; and

an electrical conductor coupling the gate electrode and the drain region.

24. The protection circuit of claim 23 wherein the metal oxide semiconductor device further comprises:

a first region of the second conductivity type formed in the second surface of the semiconductor substrate; and

a second region of the second conductivity type extending from the first surface of the semiconductor substrate into the first region.

25. The protection circuit of claim 20, wherein the transistor includes an insulated gate bipolar transistor having a second conduction terminal coupled to a second node.

26. The protection circuit of claim 25 wherein the insulated gate bipolar transistor comprises:

a semiconductor substrate having first and second surfaces;

a body region of a first conductivity type in the first surface of the semiconductor substrate;

emitter regions of a second conductivity type formed in the body region;

a gate electrode formed over the first surface of the semiconductor substrate partially overlapping the emitter regions; and

a collector region of the first conductivity type formed in the second surface.

27. The protection circuit of claim 26 wherein the insulated gate bipolar transistor further comprises an electrical conductor coupling the gate electrode and the collector region.

28. The protection circuit of claim 26 wherein the insulated gate bipolar transistor further comprises an electrical conductor coupling the gate electrode and the first surface of the semiconductor substrate.

29. A protection circuit, comprising:

a utilization circuit (2)having an input coupled to receive an input signal at first and second nodes; and

a protection circuit (41)coupled to the first and second nodes to substantially limit the input signal between first and second levels, the protection circuit including,

(a) a first transistor having a first conductor coupled to the first node; and

(b) a second transistor having a first conductor coupled to the second node.

30. The protection circuit of claim 29, wherein the first transistor includes a metal oxide semiconductor having a second conductor coupled to a control terminal of the first transistor.

31. The protection circuit of claim 30, wherein the second transistor includes a metal oxide semiconductor having a second conductor coupled to a control terminal of the second transistor and to the control terminal of the first transistor.